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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,352	12/19/2001	Mauricio Calle	4-2-3-2	3453

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EXAMINER	
NGUYEN, BINH QUOC	
ART UNIT	**PAPER NUMBER**
2664	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,352	CALLE ET AL.	
	Examiner	Art Unit	
	Binh Q. Nguyen	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/19/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/04/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-21** are rejected under 35 U.S.C. 102(e) as being anticipated by ***Jungck et al*** the U.S. Pub. No.: (2002/0065938), hereinafter referred to as ***Jungck.***

Regarding claim 1. ***Jungck*** teaches a processor *(see Fig.7, router means processor: item "702")* comprising:

a packet analyzer *(see Fig.7, item "712")*; and

first memory circuitry *(see Fig. 7, buffer item "714" means first memory circuitry)* associated with the processor and operatively coupled to the packet analyzer *(see paragraphs 0133-0134)*; wherein the packet analyzer *(see Fig.7, item "712")* is operative to at least partially analyze one or more packets received by the processor in order to determine for a given one of the packets a portion of the packet to be stored in the first memory circuitry *(see paragraphs 0150)*, the portion of the given packet when stored in the first memory circuitry thereby being accessible for subsequent processing within the processor without requiring access to second memory circuitry *(see paragraph 0155, and see paragraph 0163, Fig.8, items "810, 812, 814, 816" means second*

memory circuitry) associated with the processor and configured to store substantially the entire given packet *(see paragraphs 0134, and 0150-0155).*

Regarding claim 2. ***Jungck*** teaches the processor of claim 1 wherein the processor is configured to provide an interface between a network from which the packets are received and a switch fabric *(see paragraph 0132, Fig. 7, and 8, item " 710").*

Regarding claim 3. ***Jungck*** teaches the processor of claim 1 wherein the first memory circuitry *(see Fig. 7, buffer item "714" means first memory circuitry)* comprises an internal memory *(see Fig. 8, SDRAM item "806 (714, 716)" means internal memory)* of the processor and the second memory circuitry *(see Fig.8, items "810, 812, 814, 816" means second memory circuitry)* comprises an external memory *(see Fig.8, item SRAM/Flash Memory "812" means external memory)* of the processor.

Regarding claim 4. ***Jungck*** teaches the processor of claim 3 wherein the portion of the packet to be stored in the internal memory comprises a designated portion of a header of the packet *(see paragraphs 0150, 0166, and 0174).*

Regarding claim 5. ***Jungck*** teaches the processor of claim 3 wherein the packet analyzer at least partially analyzes each of the packets received from a network and determines for each of at least a subset of the packets a particular portion of the packet to be stored in the internal memory *(see paragraphs 0152-0154).*

Regarding claim 6. ***Jungck*** teaches the processor of claim 3 wherein the packet analyzer is configured to utilize a value *(rule set "726" means the value)* stored in a register of the processor to

determine the portion of the given packet to be stored in the internal memory *(see paragraphs 0150-0152, and 0156).*

Regarding claim 7. ***Jungck*** teaches the processor of claim 6 wherein the register comprises one of a plurality of registers which implement a look-up table accessible to the packet analyzer *(see paragraphs 0110, 0132-0133, and 0163).*

Regarding claim 8. ***Jungck*** teaches the processor of claim 7 wherein the look-up table includes a plurality of entries, each of at least a subset of the entries including packet categorizing information and an associated number of blocks of the packet to be stored in the internal memory *(see paragraphs 0094-0095, 0147-0152).*

Regarding claim 9. ***Jungck*** teaches the processor of claim 8 wherein the packet categorizing information comprises a port number specifying a port associated with the processor at which one or more of the packets may be received *(see paragraphs 0081-0082, 0178, and 0192).*

Regarding claim 10. ***Jungck*** teaches the processor of claim 8 wherein the packet categorizing information comprises a packet identifier specifying a particular packet flow *(see paragraphs 0076, 0081-0082, 0095, and 0149).*

Regarding claim 11. ***Jungck*** teaches the processor of claim 8 wherein the associated number of blocks comprises a predetermined number of blocks indicating for the given packet that substantially the entire packet is to be stored in the internal memory *(see paragraphs 0132-0134, 0166-0169).*

Regarding claim 12. ***Jungck*** teaches the processor of claim 6 wherein the stored value is updatable for each of at least a subset of the packet in a sequence of the received packets *(see paragraph 0189 rule set "726" means the value).*

Regarding claim 13. ***Jungck*** teaches the processor of claim 6 wherein the same stored value is utilizable for multiple ones of the received packets to determine corresponding portions of the multiple packets to be stored in the internal memory *(see paragraphs 0133-0134, and 0150- 0152, rule set "726" means the value).*

Regarding claim 14. ***Jungck*** teaches the processor of claim 6 wherein the value *(rule set "726" means the value)* stored in the register *(rule processor "726" means a register)* is storable therein under control of a host processor operatively coupled to the processor *(see paragraphs 0150-0155).*

Regarding claim 15. ***Jungck*** teaches the processor of claim 14 wherein the host processor is coupled to the processor via a peripheral component interconnect (PCI) bus *(see paragraph 0159, and see Fig.8, "items "828").*

Regarding claim 16. ***Jungck*** teaches the processor of claim 3 further comprising a register *(rule processor "726" means a register)* which under control of the packet analyzer *(see Fig.7, item "712")* stores packet categorizing information for the given packet and a corresponding indication of the portion of the packet to be stored in the internal memory *(see paragraphs 0150-0155).*

Regarding claim 17. ***Jungck*** teaches the processor of claim 3 further comprising a memory controller *(see Fig. 8, item "832" management controller means a memory controller)* operatively

coupled to the packet analyzer, the memory controller controlling the storage of the portion of the given packet in the internal memory *(see paragraphs 0150, 0159, 0166, and 0174).*

Regarding claim 18. ***Jungck*** teaches the processor of claim 1 wherein the processor comprises a network processor *(see Fig. 8, items "804", and "810").*

Regarding claim 19. ***Jungck*** teaches the processor of claim 1 wherein the processor is configured as an integrated circuit *(see paragraphs 0110, and 0226, chip means integrated circuit).*

Regarding claim 20. ***Jungck*** teaches a processing system *(see Fig. 7, router "702" means processing system)* comprising:

a processor *(see Fig. 8, item "842")*; and

an external memory operatively coupled to the processor *(see Fig. 8, item "840" or "812")*;

the processor further comprising:

a packet analyzer *(see Fig. 8, item " 804(712)*; and

an internal memory operatively coupled to the packet analyzer *(see Fig. 8, item SDRAM "806 (714, 716)"and paragraph 0154)*;

wherein the packet analyzer is operative to at least partially analyze one or more packets received by the processor in order to determine for a given one of the packets a portion of the packet to be stored in the internal memory *(see paragraphs 0150, and 0156)*, the portion of the given packet when stored in the internal memory thereby being accessible for subsequent processing within the processor without requiring access to the external memory, the external memory being configured to store substantially the entire given packet *(see paragraphs 0150-0156).*

Regarding claim 21. ***Jungck*** teaches a method for use in processing packets in a processor *(see Fig. 7, Router "702" means processor)* the method comprising the steps of:

at least partially analyzing one or more packets *(see Fig. 7, Packet "704")* received by the processor *(see Fig. 7, Router "702" means processor)* in order to determine for a given one of the packets a portion of the packet to be stored in first memory circuitry associated with the processor *(see paragraphs 0150-0156)*; and

storing the portion of the given packet in the first memory circuitry *(see Fig. 7, buffer item "714" means first memory circuitry)*, the portion of the given packet thereby being accessible for subsequent processing within the processor without requiring access to second memory circuitry *(see paragraph 0155, and see paragraph 0163, Fig.8, items "810, 812, 814, 816" means second memory circuitry)* associated with the processor and configured to store substantially the entire given packet *(see paragraphs 0134, and 0150-0156).*

Contact Information

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh Q. Nguyen whose telephone number is 571-272-8563. The examiner can normally be reached on M-F: 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patent Examiner:

Binh Q Nguyen
09/08/2005

WELLINGTON CHIN
SUPERVISORY PATENT EXAMINER